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Super Gate Turn-Off Thyristor

by Timothy E. Griffin

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A Super Gate Turn-Off Thyristor (SGTO) of silicon is intended for pulse applications. Its operation is discussed, and the device was turned off at low continuous current. From a review of GTO turn-off gate drivers, we discuss gate drivers for the modest continuous currents of the SGTO.

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1. Introduction

The Super Gate Turn-Off Thyristor (SGTO) is a high current pulse thyristor designed for rapid turn-on and high dI/dt to 30 kA/μs. This device is designed to deliver pulses of a finite length of time as at <1% duty cycle; see table 1 for total pulse action. The SGTO specifies turn-off current gain of <1 at <100 A for an I_{Gate} pulse of 1 μs, so the gate drive I_G must be at least as large as I_{Anode} was before turn-off. This paper summarizes the SGTO operation characteristics and design, the turn-off performance with our driver, and gate driver with ESL.

Table 1. Rated SGTO action I^2t (thousand A^2s).

pulse width (μs)	1 pulse	100 pulses	10^4 pulses	10^5 pulses
0.2	10	10	3	3
1- 1000	30	18	9	6
10,000	70	40	20	10

2. Specifications of SGTO

The SGTO Solidtron CCSTA14N40 from Silicon Power Corp. (SPCO) is for current pulses, self-dissipating above 100 A. It is designed to rapidly turn on a fast-rising output of 10-kA peak I_A brief pulses. Appropriate mounting of the SGTO package and low duty cycle are required to cool down to 25 °C before each discharge. The SGTO is specifically designed for the action per pulse at the finite number of pulses in table 1 for 25 °C before each discharge event.

We assume the power loss is mostly ohmic-like proportional to I^2, and the power loss multiplied by the pulse width is the conduction energy dissipated in the SGTO per pulse. Thus, we partly relate this action to the conduction energy dissipated. The rated action increases very gradually with the pulse width since (we assume) heat energy has more time to conduct very gradually further. The rated action decreases as approximately the logarithm of the total number of pulses increases; we assume that damage accumulates.

Data sheet specifications in table 2 were mostly maxima.

Table 2. SGTO specifications.

V_{AK} blocking (V_{GK} = 0 V)	at 25 °C >4000 V at I_A = 1 mA at >85 °C >2000 V
peak reverse V_{AK}	–5 V
I_A	continuous 100 A 10 μs pulses: repeated 10 kA, single peak 14 kA, dI/dt <30 kA/μs
I_{AK} off-state (V_{GK} = 0, V_{AK} = 4000 V)	25 °C typical <50 μA, max 100 μA 125 °C typical 100 μA, max <800 μA

I_G turn-on threshold (I_{AK} = 1 mA, R_{GK} 10 Ω, 1 µs)	5 mA
V_{AK} at 25 °C	at 10 A 0.85 V, at 50 A 1 V, at 400 A 1.6 V
dV_{AK}/dt	<1 kV/µs
I_G turn-off pulse width for 100 A	1 µs

That I_G turn-off is inconveniently narrow and therefore fast rising and falling. V_{AK} blocking would be reduced by self-heating and by military 125 °C ambient. Turn-on delay was 0.2 µs. The dV_{AK}/dt withstood without retrigerring is at least as good as usual GTOs. Reverse V_{GK} must be within –9 V; they recommend –8 V.

To keep the SGTO conducting we observed no minimum latching I_A or following/back-porch I_G. With V_{GK} = 0 V we measured at V_{AK} = 1946 V unencapsulated leakage 108.8 µA and at 4 V 41.6 µA. The data sheet represents circuit loads as small (90 nH and 0.03 Ω). Other GTOs have more turn-off current gain, around 2 to 3.

3. SGTO Pulse Literature

Others discharged eight SGTOs in short pulses (*1*), two in series of groups having in parallel two identically inductive SGTO series pairs and a 1-MΩ resistor. The current pulse had a fast rise and then decayed (without turn-off) in the capacitor-discharge ring-down circuit with small ESL load. Each SGTO had dI_A/dt to 3.12 kA/µs and a current pulse width 100 to 120 µs at 6 kV. For a 0.5-V, I_G = 0.5-A turn-on pulse, a SGTO reached full conduction rapidly and uniformly because of the 10-µm gate structure. After one pulse per minute for 1000 shots, then at 1 Hz, a three-pulse burst every minute for 1000 pulses, the pulse shape changed only 1% which demonstrated durability.

A pulse can be large; two anti-parallel SGTOs with integrated gate driver conducted >16 kA for 200 µs at low repetition rate, or 800 A root mean square (rms) for 1 s, or continual 62.4 A rms rising by 60 °C. I_G > 0.1 A gave turn-on in 1 to 5 µs, and the SGTO had effective resistance 3 mΩ cm^{-2} with low ESL. A circuit of 3 kV, 10,000 µF, 0.4 µH and 1 mΩ including parasitics discharged by eight SGTOs in parallel gave a half-sine 450 kA 200 µs long with junction rising by 95 °C (*2*). Discharging 200,000 µF through a load 25 nH with 6.5 mΩ, each of 12 SGTOs in parallel reached 37.5 kA at 9 kA/µs in a more square-rising pulse. Reliability (*3*) comes from faster turn-on by SGTO fine gate structure and from thinPak absence of wire bonds.

4. Design of SGTO

The SGTO has a *p* type silicon (Si) bottom anode, then a thick drift layer *n*, then gate *p*, then top cathode *n*. The package base is aluminum nitride (AlN) clad with 0.1 cm cubic (Cu) and withstands thermal cycling (*2*). A perforated, metallized ceramic substrate is attached to the bottom of the Si with 302 °C solder (*2 and 4*). For the top, very narrow emitter fingers and dense emitter structure along those fingers need thinPak packaging. This has a ceramic lid of alumina or AlN (oversized to protect the chip edges sealed with underfill) with two-sided patterned Cu and plated-metallized vias; each of many gate contacts covers a small cell. A 280 °C solder bonds the lid to the chip; then 180 °C solder is on the outer surface of the lid and the rear of the chip. There is low and uniform impedance of gate to cathode and the lid has similar for contacts to them, which notably improved both turn-on and turn-off switching while reducing V_f to that of a 5 kV *p-i-n* diode.

The SGTO area is 2 cm^2 active and 3.3 cm^2 total with 160,000 emitter island cells on 0.0660-cm-thick, 450 Ω-cm starting Si of 4700 V breakdown (5500 V if 750 Ω-cm) (*2*). To get a low voltage drop, modified gettering gives acceptable turn-off I_G, turn-off stability, and high carrier lifetime. In pulses of small percent duty cycle, turn-off claims >1000 A cm^{-2}. Turn-off time limits SGTO performance in a DC-to-AC inverter to an output sine <60 Hz. Turn-on is determined by R_{GK}, especially if <100 Ω, and without R_{GK} it requires about 1 mA. For the V_{GK} = 2 V recommended turn-on, 10 Ω would require 40 to 50 mA.

Turn-off is low priority in the SGTO's design; the supply must be less than several hundred volts to have a wider undepleted base with adequate series impedance to keep current uniform during turn-off (*2*). V_f is low from the upper base being 16 times thinner at 6 μm and its charge 7 times lower at 2×10^{13} cm^{-2}, so the upper base V_f is that of a diode and the upper transistor (equivalent) gain α_1 is nearly 1. Lowered V_f and improved heat removal permits twice the current density. For definite latch on α_1 + lower transistor gain $\alpha_2 \geq 1.1$, permitting α_2 as low as 0.1; carrier lifetime is reduced by irradiation. These give 1/4 to 1/6 the switching losses, permitting 4 to 6 times the frequency. The SGTO switches 2000 V and 200 A with effective turn-off time 0.75 μs and turn-off loss of 0.3 J. We note with decreased current that this loss does not decrease as rapidly and would be a high 150 W at 500 Hz so we de-emphasize continuous switching. The older and present SGTO effective turn-off times were 4.7 μs with V_f = 1 V at 100 A cm^{-2}, 1.2 μs, and 0.7 μs with 1.53 V.

5. Some Thermal Considerations

The SGTO package was highly thermally conductive but only 1.45 cm by 2.2 cm by 0.15 cm thick, slightly larger than the chip. Heat removal was mostly downward, improved by a solid internal bottom interface and by superior heat spreading (*2*), but was denser since it was over the smaller-than-conventional areas of the chip and package. The SGTO chip was not thinned. Within 10 years, thyristors of SiC would be an improvement.

6. Gate Driver Trigger Transformer

We contacted a SGTO with alligator clips; polytetrafluoroethylene pads insulated the package from unwanted contact. The package front had three metal stripe contacts 2 cm long; the center 0.25 cm wide contact was the gate. The outer two 0.32 cm wide contacts were the cathode, one was our power contact and the other the return for turn-on and turn-off. Each stripe has several spots of solder; to contact them, the data sheet mentioned 63% Sn- 37% Pb solder, but even with RMA flux, this could not give us meaningful adhesion of soldered wire.

From trigger transformer VishayDale DALPT020BH106 two outputs in parallel gave equivalent 1 Ω in series with 100 μH, large so calculated to give 1.4 A. An input of 8 V was switched by an nMOS IRF540N. The transformer input had an anti-parallel diode MUR4100E, and the output went through another MUR4100E to the SGTO gate. A trigger transformer or optocoupler would isolate input voltage for V_K >0 V. Experimentally, our turn-off trigger transformer gave too little current, had inductance to make it end with ringing to positive V_{GK}, and was slow so we rejected it.

As a turn-off driver, optocoupler Agilent HCPL-3180 has too low a duty cycle of low output current at too much variation of effective internal series resistance and voltage drop. As a turn-on driver at low current, it has too large a variation in output voltage which requires a supply far exceeding 2 V. At V_{CC} –4 V the specified I_{out} is >0.5 A, at V_{CC} –10 V it is >2 A for <10 μs and <0.2% duty cycle, and at typical V_{CC} –2 –1.3I_{out} it is I_{out}.

R_{GK}, initially 20 Ω, in parallel with V_{GK} stabilized it but took some of the gate driver's current from I_G. We changed to an R_{GK} of 10 Ω suggested for high temperature and/or noisy environment.

7. Gate Driver with negative Metal Oxide Semiconductor and positive Metal Oxide Semiconductor

We experimentally turned on the SGTO through an negative metal oxide semiconductor (nMOS) and turned it off through a positive metal oxide semiconductor (pMOS). For turn-on, although 1 V worked, a HP6227B power supply at 2 V stiffened by a 0.47-μF polystyrene capacitor went to the drain of an nMOS IRF540N. A HP8116A signal generator's 15 V pulse for 2 μs went through a 25-Ω resistor to the MOS gate with its ground not connected to the MOS source; the 15 V was greater than the MOS source's potential could be for more than a fraction of a microsecond. This produced a turn-on I_G of 80 mA for 1 μs.

For SGTO turn-off, the stiffening capacitors for an Agilent E3614A power supply at –8 V provided I_G during the rise time, and thus need enough capacitance working to a frequency around $3/t_{\text{rise time}}$. Polypropylene capacitors with planar leads would have helped that. Two 10-μF Cornell-Dubilier 935C4W10K (capacitance goes through 0 at 216 kHz) were in parallel with three ceramic 0.1 μF capacitors (capacitance goes through 0 at 2.4 MHz). The supply went to the drain of a pMOS Fairchild FQI7P20TU which specifies a turn-on rise time 110 to <230 ns and source-drain resistance <0.69 Ω. A HP8116A through a 50-Ω resistor drove the pMOS gate. To block ringing of current into the SGTO gate, a Schottky 1N5822 had its cathode attached to the pMOS source and its anode to the nMOS source; from there, turn-off I_G initially went through a 0.5-Ω resistor (to try to reduce ringing) to the SGTO gate.

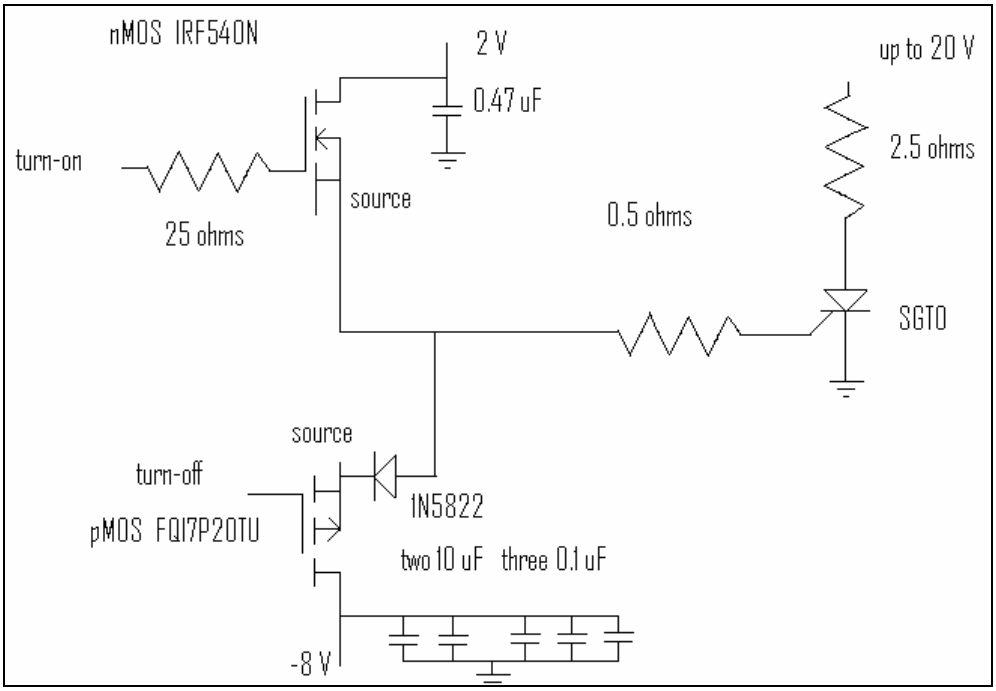

Figure 1. SGTO gate drivers.

Our SGTO power supply Agilent E3633A went through a planar load of 2.5 Ω and near 80 nH to the SGTO anode. Cu strip conductor soldered to the Ohmite TA1K0PH2R50K load's screw terminal posts would have reduced the ESL and ESR. The SGTO turned off 5.8 A from the power supply at 20 V and was usually fan cooled.

Turn-off required our >1.4 ms SGTO gate pulse. During a pulse, the voltage at the pMOS drain dropped from –8 V to –4 V in about 80 ns; adding a ceramic 0.01 µF capacitor (capacitance goes through 0 at 10 MHz) did not help significantly. Breadboard spring-loaded connections did not optimize stray inductance. With a 0.5-Ω driver resistor to the SGTO gate, the I_G reached an initial –6.8 A peak in 3 µs. On a few turn-offs, 1-MHz ringing was observed or a failure to turn off.

Our turn-off pulse width >1.4 ms (1.7 ms for a warm SGTO) was slower than useful. With R_{GK} = 10 Ω I_G with no resistance in series peaked at –10.2 A. Turn-off I_G peaked to –10 A at 4 µs and by 700 µs slowly declined to around –0.57 A; so to 191 µs the total turn-off gate charge Q_{GQT} was 590 µC (turn-off charge Q_{GQ} is I_G integrated only to the peak). $V_{pMOS\ drain}$ at the capacitors went from –8 V to –4 V (I_G = –0.24 A) in 0.12 µs and first rang through –8 V much later at 13 µs.

We tried IRF9540N pMOS rated R_{ds} = 0.117 Ω and turn-on rise time at 67 ns. With no resistance between driver and SGTO gate, I_G peaked at –12.4 A but there were no other significant improvements.

8. Ordinary GTO Driver and Turn-Off

A turn-off driver's I_G output path including capacitors needs low ESL and fairly low ESR. Better than larger diameter capacitor leads are the 1.5-cm-wide planar leads of the last two in table 3.

Table 3. Polypropylene capacitor performance.

Cornell-Dubilier part number	**(µF)**	**(V)**	**ESR (mΩ)**	**ESL (nH)**	**d*V*/d*t* (V/µs)**	**(A rms)**	**C goes through 0 at (kHz)**
940C6W4P7K	4.7	600	4	38	105		321
940C20W1K	1	2000	5	42	754		697
SCD475K601A3Z25	4.7	600	4	<20	250	46.2	384
SCD105K202A3Z25	1	2000	6	<20	600	21.3	

To reduce ESL, a gate driver circuit board would have careful layout close to the gate. From the power supply, fairly wide Cu traces carrying I_G would locate each outgoing trace over its return trace separated by a very thin insulator in a strip line, avoiding coaxial cable and definitely twisted pair. From a 20-V supply with a 470-µF electrolytic capacitor (too slow for SGTO), an

ordinary path went through a MOS (5); 10 parallel paths to reduce ESL reported turn-off dI_G/dt merely 220 A/μs. This 20 V was reduced in series after the supply capacitor's ESR and 5 nH to 18.9 V, after the MOS to 18.7 V, after the printed circuit board ESR and 15 nH to 15.4 V, the cable's 25 nH to 9.9 V, and the lem connector's ESR and 25 nH (total <65 nH) to only 4.4 V signal into the ordinary gate's ESR and 20 nH.

9 Conclusions for SGTO and Gate Turn-Off

The SGTO is a high current pulse thyristor designed for rapid turn-on. The design of this device makes it unsuitable for continuous switching because of a turn-off gain <1, turn-off current <100 A, performance at too low a frequency for a DC-to-AC motor inverter and significant density of heat dissipation.

Preferred for turn-off uniformity is a power supply of less than several hundred volts. The SGTO had low V_f, low turn-on switching losses per unit area for high-current pulses and improved cooling per unit area. A 1 μs turn-off I_G pulse needs a driver with strictly minimized ESL.

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